Superconducting Chip Fabrication Yield Improvement

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Abstract: Cat qubits can alleviate the hardware burden for logical qubits by passively correcting bit-flip errors via two-photon dissipation. However, to properly harness this potential, effective control of the circuit's Josephson Junctions (JJs) is essential. Dolan-technique fabricated JJs geometry can be affected during fabrication by multiple factors like uneven oxidation, lithography problems or the bilayer (LOR/PMMA) thickness. During this work two different projects were developed to improve the cat-qubit fabrication yield: First, a non-invasive optical characterization methodology based in ellipsometry was developed for accurately measuring LOR and PMMA uniformity across the wafer. It was seen that by characterizing the film near the Brewster angle and correcting for the optical properties of the substrate, an offset from the real LOR and PMMA film thickness of 8.7 and 5 nm was obtained, respectively. Second, a post-fabrication inductance tuning by thermal treatment method was developed. This process was able to correct up to 20% inductance error, depending on the junction area and baking temperature, with an error on the predicted resistance change lower than 1.2%.

References:

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