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Ultra-thin Layer Transfer Technology in 3DIC

This study introduces a groundbreaking SOI-based temporary bonding technique for dual-layer active devices, addressing significant challenges in thermal management and interlayer alignment. Through optimized bonding, grinding, CMP, and wet etching, we successfully transferred an 8-inch, 2-micron-thick high-quality device film and stacked it onto another device wafer, ensuring good electrical performance in both layers. This platform achieves interlayer thickness below 1 μm, allowing precise visible-light alignment and enabling more flexible 3DIC circuit designs, including the potential for quantum device stacking or interposer preparation.