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Hardware-efficient quantum error correction using concatenated bosonic qubits

To solve problems of practical importance, quantum computers will likely need to incorporate quantum error correction, where a logical qubit is redundantly encoded in many noisy physical qubits. The large physical-qubit overhead typically associated with error correction motivates the search for more hardware-efficient approaches. In this talk we will present and characterize a superconducting circuit which realizes a logical qubit memory formed from the concatenation of encoded bosonic cat qubits with an outer repetition code of distance $d=5$. The bosonic cat qubits are passively protected against bit flips by two-photon dissipation. The phase-flip correcting repetition code operates below threshold, with logical phase-flip error decreasing with code distance from $d=3$ to $d=5$. Concurrently, the logical bit-flip error is suppressed with increasing cat-qubit mean photon number. The minimum measured logical error per cycle is on average 1.75(2)% for the distance-3 code sections, and 1.65(3)% for the longer distance-5 code. We will tie our results to the longer term opportunities for reaching computationally relevant error rates with concatenated bosonic qubits.